

**TSMC 28nm Analog and Mixed-Signal Reference Flow Includes Silicon
Frontline’s F3D Parasitic Extraction Software**
Nanometer designs require 3D field-solver accuracy

Campbell, CA – June 10, 2010 – Silicon Frontline Technology, Inc. (SFT), the silicon-proven, full-chip, field-solver company, announced today that its **F3D (Fast 3D)** parasitic extraction software for post-layout verification, has been selected as part of TSMC’s 28 nanometer (nm) Analog and Mixed-Signal (AMS) Reference Flow 1.0. F3D was chosen because it offers parasitic extraction with guaranteed accuracy along with the capacity and performance to handle large nm designs.

“We are pleased to have the world’s leading foundry, TSMC, select our 3D extraction software for their 28nm AMS Reference Flow,” remarked Yuri Feinberg, CEO. “With F3D, TSMC’s customers can achieve guaranteed accuracy and take advantage of our full-chip capacity and exceptional performance.”

“TSMC collaborates with select EDA suppliers like Silicon Frontline to get design tools ready for our most advanced semiconductor processes,” added Tom Quan, deputy director, design methodology and service marketing at TSMC. “Silicon Frontline’s 3D extraction software has been one of the first EDA tools to be included in our 28nm AMS Reference Flow”

Last year, [TSMC](#) validated Silicon Frontline’s F3D product for 40- and 65-nanometer design technologies for its iRCX support

The Importance of Guaranteed Accuracy, Performance

The demand for higher performance and reliability for designs targeting nanometer process nodes drives the need for parasitic extraction accuracy. Analog, AMS, and embedded memory designs require extraction software that delivers 3D field-solver accuracy, since small coupling capacitances can very often be the cause of failure.

Silicon Frontline's post-layout verification software offers accuracy and high performance based on its proprietary and rigorous 3D technology to extract parasitics. Users specify the level of accuracy desired, net by net, at the block level or with regular expressions. In this way, the resulting parasitics are guaranteed correct within the specified accuracy.

Silicon-Proven Technology

Since Silicon Frontline's [introduction](#) last year, the company's 3D technology has been endorsed by the world's leading foundries, its customers include eight of the world's top 25 semiconductor companies and its software has been used to verify over 200 designs.

About Silicon Frontline

[Silicon Frontline Technology](#), Inc. provides post-layout verification software that is *Guaranteed Accurate* and works with existing design flows from major EDA vendors. Using new 3D technology, the company's software products improve silicon quality for standard and advanced nanometer processes. For more information please visit www.siliconfrontline.com. For sales or general assistance, please email info@SiliconFrontline.com or sft@marubeni-sys.com.

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