

## UMC Uses Silicon Frontline's Field Solver to Generate Reference Extraction Data

*Selection boosts customers' confidence in F3D for post-layout verification*

Los Gatos, CA – May 25, 2010 – [Silicon Frontline Technology](#), Inc. (SFT) announced today that its 3D extraction software for post-layout verification **F3D (Fast 3D)** has been qualified by United Microelectronics Corporation (NYSE: UMC, TSE: 2303) ("UMC"), a leading global semiconductor foundry, as the reference field solver for parasitic extraction.

UMC verified F3D's accuracy through extensive comparison with internal benchmarks. The reliability and repeatability of results led to UMC's adoption of F3D to generate reference data. Silicon Frontline's F3D provides field solver accuracy for full-chip design, enabling higher quality extraction and faster post-layout verification closure.

"We are excited to add F3D as another reference field solver at UMC. We adopted Silicon Frontline's F3D as a 3D extractor because it provides accuracy for many styles of circuitry, including high precision analog such as ADCs," said Stephen Fu, Director of IP Development and Design Support at UMC. "This opens the door to providing higher quality silicon to customers."

"Having UMC, a leading and well-respected silicon foundry, select F3D for generating reference parasitic extraction data boosts customers' confidence in our results," added Yuri Feinberg, Silicon Frontline CEO. "As customers experience F3D's ability to accurately match sensitive parasitics, they realize more aggressive design goals are achievable and accurate design verification is possible."

Silicon Frontline's post-layout verification software guarantees accuracy and high performance by using rigorous 3D technology to extract parasitics. Users have the option to specify the level of accuracy desired, net by net, at the block level or with regular expressions. By guaranteeing accuracy, Silicon Frontline is ensuring the resulting parasitics are correct within the user-specified accuracy.

In July 2009, [UMC](#) validated F3D for its nanometer design processes.

### **About Silicon Frontline**

[Silicon Frontline Technology](#), Inc. provides post-layout verification software that is *Guaranteed Accurate* and works with existing design flows from major EDA vendors. Using new 3D technology, the company's software products improve silicon quality for standard and advanced nanometer

processes. To date, Silicon Frontline customers are among the top 20 semiconductor companies, and the company's technology has been endorsed by a number of the leading foundries.

For more information please visit [www.siliconfrontline.com](http://www.siliconfrontline.com).

For sales or general assistance, please email [info@SiliconFrontline.com](mailto:info@SiliconFrontline.com) or [sft@marubeni-sys.com](mailto:sft@marubeni-sys.com).

**-End-**

Press Contact:

Georgia Marszalek, ValleyPR LLC, +1 650 345 7477, [Georgia@ValleyPR.com](mailto:Georgia@ValleyPR.com)

*All trademarks and tradenames are the property of their respective holders.*