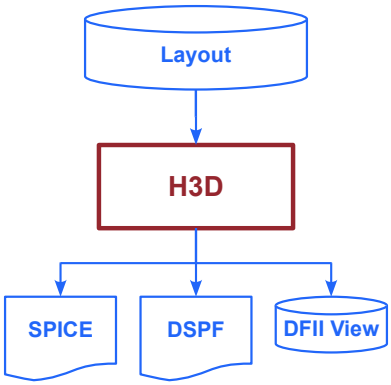
Datasheet

H3D

HIERARCHICAL 3D RC EXTRACTION

Guaranteed *FAST.* Guaranteed *ACCURATE.*

Nanometer process technologies permit designers to develop innovative circuits, delivering high-performance functionality and incorporating logic, memory, analog and RF on a single CMOS die. Too often, though, out-of-date layout verification or analysis methodologies prevent designers achieving the full capabilities of the process.



Incomplete verification coverage or inaccurate analysis force designers to add large guardbands, and to sign off with only partial layout verification completed. Performance and yield impact often require expensive silicon debug, redesign and respins to repair.

For designers tired of the constraints forced on them by inefficient and inaccurate layout verification, H3D is a hierarchical extraction tool, delivering superior sub-linear performance, with guaranteed 3D accuracy, for full-chip verification.

Compared to traditional tools that require designers to compromise coverage and precision, H3D delivers full-chip guaranteed accuracy, permitting stringent schedules to be met with confidence.

FEATURES

- Superior performance, independent of net size or geometry; scalable with compute hardware
- 3D-accurate, using proprietary floating random walk algorithm
- Unlimited capacity for full-chip full-accuracy extraction
- Supports industry-standard back-end flows
- Flat or hierarchical data in; hierarchical post-layout extracted netlist out

BENEFITS

- Breakthrough performance makes possible full-chip extraction & analysis with 3D accuracy
- 3D field solver accuracy; faster than 2.5D pattern-matching performance on large hierarchical circuits
- Breaks the bottleneck of flat post-layout analysis, enabling a hierarchical flow from schematic to sign-off
- Full-chip capacity eliminates netlist cutting and stitching
- Supported for advanced nanometer processes from leading foundries ensures successful sign-off to tape-out

SPECIFICATIONS

Supported Flows

- Annotated GDSII
- Mentor Graphics Calibre CI
- Cadence DFII
- Synopsys Milkyway / Hercules

Data Output Formats

- Netlists containing distributed or lumped C, R, RC or RCC data
- Flat or hierarchical SPICE netlist
- Flat or hierarchical DSPF
- DFII Extracted View (for Cadence ADE)

BUILDS ON SOLID F3D FOUNDATION

Silicon Frontline's F3D extraction tool is industry-proven, verifying several hundred designs since launch. F3D offers precise extraction of advanced manufacturing effects, including metal filling and slotting; non-conformal dielectrics; per-layer biasing; temperature-dependent metal parameters, and OPC, RET, CMP and etch effects. In addition, support for next-generation active and passive devices is standard.

HIERARCHY FROM SCHEMATIC TO SIGN-OFF

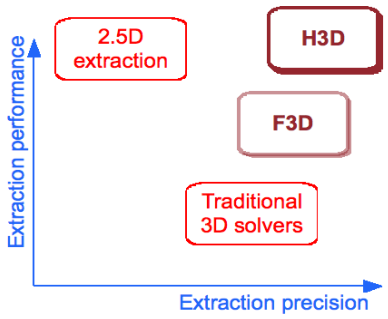
Traditional extraction tools produce a flat post-layout netlist, which for circuits of any complexity is too big to simulate or perform any meaningful analysis. With H3D maintaining or rebuilding hierarchical structure, designers can now produce a post-layout netlist that mimics exactly the pre-layout structure they introduced. Accurate, fully-extracted post-layout simulation now becomes a possibility.

GUARANTEED FAST AND GUARANTEED ACCURATE

H3D offers user-selection for accuracy on a signal net or design block basis, and this level of accuracy is guaranteed to be achieved. Performance can then be optimized across the circuit, both by varying desired accuracy and by increasing the number of concurrent extraction jobs.

PERFORMANCE

H3D offers extraction at 3D precision with performance superior to 2.5D, independent of net size, given a hierarchical structure and appropriate compute resources. Also, users optimize run-time by selectively trading off performance and precision. Finally, performance is improved linearly with addition of CPUs.



Circuit	# MOS	# Nets	Process	F3D runtime	H3D runtime	Speed Up
512w16b	62607	20129	65nm	37.9 hrs	1.35 hrs	28.0
256w2b	6234	2027	65nm	2.63 hrs	0.26 hrs	10.1
64x128_rfG40	93467	43067	40nm	45.7 hrs	0.52 hrs	88.0
64r72c	27920	12172	28nm	10.5 hrs	0.21 hrs	50.0
sj4096x	4.5M	3.2M	40nm	180 hrs	1.5 hrs	120.0
ddtop	8.5M	1.9M	55nm	336 hrs	30 hrs	11.0

CONTACT INFORMATION

Silicon Frontline Technology, Inc.
595 Millich Drive, Suite 206
Campbell, CA 95008

Tel: +1 (408) 963-6916
Fax: +1 (408) 963-6906
info@siliconfrontline.com