Introduction
Today’s advanced process technologies create reliability challenges for designers, especially for highly-integrated circuits. Thinner gate oxides and wires coupled with multiple power domains, significantly increase the impact of ESD. Failures are most often only identified in silicon testing, leading to re-designs and re-spins.

ESRA (Electrostatic Reliability Analysis) provides a full-chip ESD analysis solution. It delivers extraction, analysis and debugging capability in one integrated environment with the capacity to analyze the full chip. Highlighted violations permit designers to perform corrections at any time in the design process.

ESRA builds on production-proven Silicon Frontline technologies, including fast and guaranteed accurate parasitic extraction and circuit-proven, high-capacity matrix solvers.

Layout based, full-chip visualization and debugging of current density and potential distribution is included, and the whole solution is seamlessly integrated within existing layout flows.

Features
- Layout based ESD network verification with cell, block, full chip and package level analysis
- Capacity and performance to verify unlimited size designs including multiple pads, nets and ESD Devices
- Resistance calculation: pad-to-pad, between groups of pads and “loop resistances”
- Automated identification and detailed reporting of the least resistive path (or several paths) involving many nets, ESD devices, and pads
- Hierarchical debugging provides telescopic and microscopic views of design for faster debug
- Handling of HBM, MM, and CDM ESD events
- Interactive GUI-based visualization highlights problems related to excessive resistance, current density, and voltage drops
- Works on both Pre- and post-LVS clean designs
- Performs analysis on cell, block, or full chip level
- Includes analysis of electrical connectivity at the package level
- Ensures efficient and quick capture of typical layout mistakes:
  - Inefficient connections of pads to power nets
  - Insufficient metal line width
  - Missing vias or contacts
  - Non-strapped metal lines
  - Unbalanced current routing in ESD cells
- Integration into existing post-layout verification flows; be productive with fast, accurate analysis.

Benefits
- ESRA automates verification of ESD protection networks for electrical connectivity, resistance, and current density checks
- Replaces manual ESD checks with well defined automated checks
- ESRA offers a new verification methodology that quickly identifies issues in the layout, and analyzes weak elements of ESD network
- A detailed (mesh-based) simulation and analysis of ESD protection devices and network elements, ensures the efficiency of electrical connections, and their compliance with current density and resistance rules
- Early capture of ESD protection problems avoids expensive silicon re-designs and re-spins.
Introduction

ESD cells and devices – diodes, transistors, clamps, etc. – consist of a large number of elementary devices that are interconnected by metal layers, to provide sufficient ESD protection. Detailed understanding of the current flow and potential distributions in these interconnects and devices is important to optimize the device layouts and to ensure a balanced current distribution, low resistance, and efficient connection of devices to power nets. Standard parasitic extraction and simulation approaches are inadequate to describe these effects, and ESRA Device Analysis option is filling this gap.

Features

- Accurate handling of complex non-Manhattan geometric shapes and 2D/3D current spreading and crowding effects
- Provides current density details down to individual via, contact, and 2D/3D metal shapes
- GDS or CCI layout input
- Simulation of distributed current flow in ESD device elements
- Capturing complex interactions between ESD cells and their interconnect environment
- GUI visualization of current densities and potential distributions, with highlighting of high current density areas

Benefits

- Detailed 3D simulation of current flow in ESD protection devices with a focus on interconnect analysis and optimization
- Resistance calculation, accounting for distributed device and interconnect resistance
  - Allows for design of lowest resistance
  - Provides method to obtain uniform current distribution through device(s)