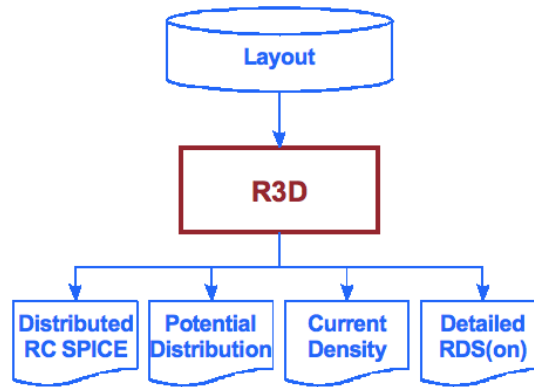


Power transistors are ubiquitous in modern electronic devices, from power supplies and DC-to-DC convertors, to power and motor control and servo applications. A critical factor that determines efficiency and reliability is the transistor on-state resistance RDS(on) comprising several resistive components, from substrate to source diffusion. Optimizing the resistance of this metal interconnect brings enormous benefits by improving efficiency and battery life through reduced losses, reducing temperature, and extended reliability.

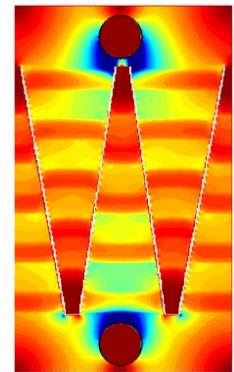
Currently, device engineers optimize these metal interconnects through time-consuming and expensive empirical methods, building and attempting to analyze test structures. This is a huge challenge, given the large and complex multi-layer metal geometries, composed of a huge number of small yet significant geometries, resulting in complicated non-uniform currents flowing in and between metal layers.

R3D is a resistance extraction and analysis tool



targeted to these power devices. By combining a uniquely powerful geometry processing engine with a highly efficient iterative matrix solver, R3D simulates complex current flows, and potential distributions. Extracting an RC distributed netlist of the complex gate structures allows dynamic

simulation and analysis of the precise device operation, including switching losses, and how current densities affect device reliability. R3D precisely simulates lateral current flow in metal layers and vertical current flow in vias and contacts, and the effects of active device conductance. Results include detailed RDS(on) data, the electrical resistance of source and drain interconnect structures; electric potential and current density distributions; all currents through vias and active device elements.



Complex current density analysis

## FEATURES

- Advanced 3D extractor and solver for source, drain interconnect structures, including multi-port to multi-port analyses
- Extracts distributed RC SPICE netlist for gate structure, enabling precise transient simulation of gate operation
- Precisely solves electric potential distributions and current densities for all metal layers
- Calculates total current and resistance of entire interconnect structure
- Applicable to any power device array types (MOSFET, BJT, etc)
- Powerful data visualization for post-processing saved simulation results

## BENEFITS

- Fast, accurate and efficient handling of even very large and complex designs
- Powerful results visualization of conductances, current and potential distributions and densities
- Enables interconnect resistance optimization and sensitivity analysis
- Drives optimal wire bond pad placement and configuration
- Improves reliability through current density and electromigration analysis, and hot spot analysis
- Guides users to rapid problem identification (e.g. "metal debiasing" and "scaling") and prompt resolution

## SPECIFICATIONS

### Supported Flows

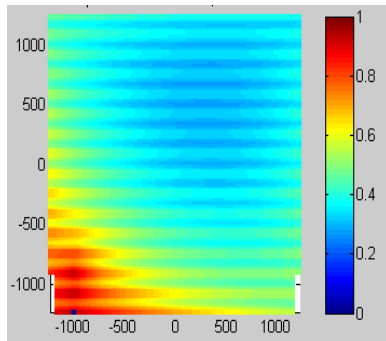
- Annotated GDSII
- Mentor Graphics Calibre CI
- Cadence DFII

### Data Output Formats

- Distributed RC SPICE netlist
- Current density
- Electric potential distribution
- Detailed RDS(on) data

## RAPID DESIGN OPTIMIZATION

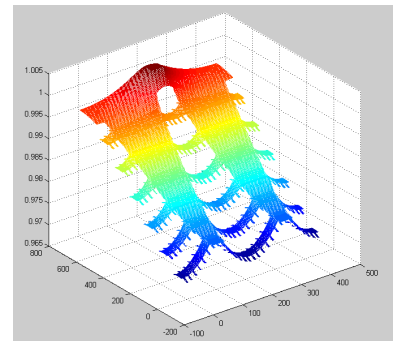
The high-throughput simulation engine permits efficient design parameter optimization, including bond wire placement and configuration; number of metal layers; metal layout, including complex slotting; and placement of sensor device, etc. With R3D, device engineers can analyze many more layout alternatives, without needing to make expensive test structures. With R3D better designs get to market sooner.



Complex gate  
frequency response

## BREADTH OF ANALYSIS OPTIONS

In addition to resistance, current and electric potential analysis, R3D permits sensitivity, current density and electromigration, and hot spot analyses. By providing a deep physical insight into the operation of the interconnect structure, R3D empowers process development, device and design groups to design, simulate and optimize power arrays without manufacturing iteration.



Electric potential  
M1-M4 layer distribution

## CONTACT INFORMATION

Silicon Frontline Technology, Inc.  
595 Millich Drive, Suite 206  
Campbell, CA 95008

Tel: +1 (408) 963-6916  
Fax: +1 (408) 963-6906  
info@siliconfrontline.com

Silicon Frontline Technology, the Silicon Frontline logo, F3D, and R3D are trademarks or registered trademarks of Silicon Frontline Technology, Inc. All other trademarks and products are the property of their respective owners.