Datasheet

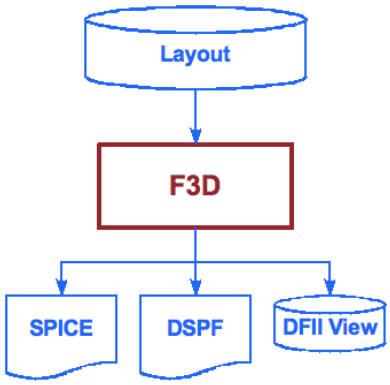
F3D

FAST ACCURATE 3D RC EXTRACTION

SILICON FRONTLINE

Guaranteed *FAST.* Guaranteed *ACCURATE.*

Today's advanced process technologies increasingly challenge designers who are developing innovative IC designs that utilize the full process capabilities. These capabilities stretch existing layout verification and analysis methodologies, forcing designers to sign-off their designs with only incomplete or imprecise coverage, impacting silicon performance and yields, and often requiring silicon re-spins to repair.



Traditional 2.5D pattern-matching extraction tools lack the precision to adequately model all required parasitic data, while 3D solvers lack the circuit capacity and performance to handle anything but the smallest structures, usually for characterization purposes only. In addition, they are difficult to configure and control.

F3D is a unique and ground-breaking layout extraction tool, designed from the ground up to deliver breakthrough levels of performance, precision and circuit capacity. It offers superior 3D precision extraction, at near 2.5D levels of performance and capacity.

Based on Silicon Frontline's proprietary technology, F3D extracts 3D capacitance and distributed RC parameters from the layout view, rigorously solving from first principles field equations and producing highly-precise parasitic data that includes all physical, optical and chemical/etching effects of leading-edge process technologies.

F3D supports industry-standard post-layout verification flows, and outputs highly-precise data for simulation and analysis. Analog, mixed-signal and advanced digital designers benefit from deploying F3D by enabling more precise timing, power, noise and other electrical verification and analyses at sign-off.

FEATURES

- Advanced 3D field solver based on stochastic random walk
- Distributed RC extraction, including all geometry-to-geometry couplings
- Best-in-class run-time performance and memory utilization, independent of net size or structure
- Extraction includes advanced manufacturing process features, including active and passive devices
- Integrated into existing verification flows; be productive immediately

BENEFITS

- Extreme extraction performance brings 3D speed and capacity to analog IC designers
- Analyze complex layout interconnect, including all advanced manufacturing effects
- User-specified extraction accuracy permits precision / performance trade-off
- Eliminate re-spins while maximizing margins, yield, and performance
- Validated support for advanced process technologies from leading foundries, including TSMC and UMC

SPECIFICATIONS

Supported Flows

- Annotated GDSII
- Mentor Graphics Calibre CI
- Cadence DFII
- Synopsys Milkyway / Hercules

Data Output Formats

- SPICE netlist, capacitance matrix
- Distributed coupled and decoupled DSPF
- DFII Extracted View (for Cadence ADE)

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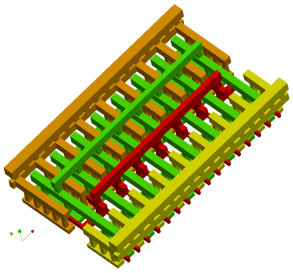
ADVANCED MANUFACTURING EFFECTS

Today's advanced manufacturing processes employ layout techniques that have impact post-lithography and during manufacturing. F3D supports extraction of data to enable modeling of these effects, including floating metal filling and slotting; use of conformal dielectric; trapezoidal wire cross-sectional shape, per-layer biasing; temperature-dependent metal resistance parameters; and many other OPC, RET, CMP and etch or lithography effects.



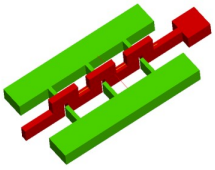
Truly capture all 3D & manufacturing effects

PRECISE CAPACITANCE EXTRACTION

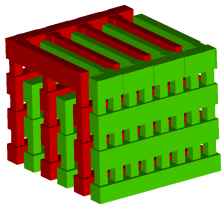
F3D is highly-accurate, extracting precise 3D capacitance values with user-specified accuracy. In addition to interconnect-to-interconnect capacitance values, F3D also extracts, under user control, device-related parasitic capacitances, including poly-to-contact; poly-to-metal; and contact-to-gate.

NEXT-GENERATION DEVICE SUPPORT

F3D supports advanced active device features, extracting all relevant data for interacting geometries, including multi-finger & multi-gate devices; FinFETs and other 3D MOS transistor structures; and devices with raised source and drain areas. Advanced passive device structures are also supported, including 3D capacitance structures such as MIM; MOM; PIP and VPP.



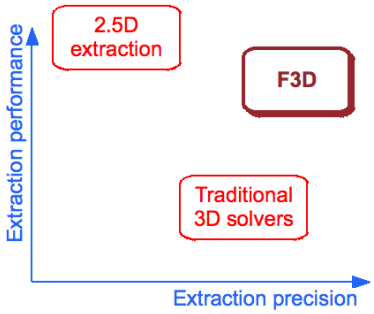
Multi-gate FinFET



MOM/VPP Capacitor

PERFORMANCE

F3D offers extraction at 3D precision with near-2.5D performance, independent of net size. Also, users optimize run-time by selectively trading off performance and precision. Finally, performance is improved linearly with addition of CPUs.



Circuit	# MOS	# Nets	Runtime (s)	Peak Mem (MB)
Divider 1	32	42	142	729
Divider 2	168	122	96	864
Analog 1	102	177	92	868
Analog 2	12	203	158	794
Analog 3	493	992	308	897
Analog 4	7322	2955	1413	8944
Analog 5	158	20903	159	1066
AMS 1	1258	10180	1250	1030
Chg pump	1512	223327	1383	3713
VCO 1	6300	231586	2579	5627
PLL 1	51150	1308750	7054	4936
SOC 1		400000	7120	

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