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Silicon Frontline Technology, Founded by EDA Technologists, Announces Post-Layout EDA Verification Software

3D technology delivers a *Guaranteed Accurate* solution for full- chip verification,
Works in existing flows, Supports today's standard and advanced nanometer processes,
Analyzes power devices

Los Gatos, CA – May 12, 2009 – Silicon Frontline Technology, Inc. (SFT), a new company founded by Electronic Design Automation (EDA) technologists, today announced the company and its first products for post-layout verification: **F3D (Fast 3D)** for fast 3D extraction and **R3D (Resistive 3D)** for 3D extraction and analysis of large resistive structures like power devices.

The products incorporate patent-pending 3D technology to deliver a *Guaranteed Accurate* solution for full-chip, post-layout verification. They work in industry standard flows allowing simpler adoption and quicker closure, with guaranteed accuracy, of the post-layout verification loop.

Silicon Frontline was founded in 2005 by EDA software and post-layout verification experts, Yuri Feinberg, CEO, and Dr. Andrei Tcherniaev, VP Engineering, who previously co-founded NASSDA (acquired by Synopsys in 2005) and were the original developers of HSIM, the EDA industry's first hierarchical circuit simulator.

"We founded Silicon Frontline with the goal of moving post-layout verification technology to the next level," said Yuri Feinberg, CEO. "We want EDA users to experience what hasn't been possible until now—Guaranteed Accuracy."

"Traditional extraction technology could not model our design with sufficient confidence. With Silicon Frontline's 3D software, we match simulations to silicon, providing us the shortest and highest confidence path to quality and reliability," remarked Patrick O'Connor, VP Engineering at Canesta, a developer of 3D image sensors.

What's New

Guaranteed Accurate Post-Layout Verification Technology

Silicon Frontline's post-layout verification software guarantees accuracy and high performance by using rigorous 3D technology to extract parasitics. Users have the option to specify the level of accuracy desired, net by net, at block level or with regular expressions.

By guaranteeing accuracy, Silicon Frontline is ensuring the resulting parasitics are correct within the user-specified accuracy.

Support for Standard and Advanced Nanometer Processes

The Silicon Frontline software has been qualified by major foundries for accuracy, performance, and capacity as well as integration with major physical verification systems. It can be used with today's mature process technology or advanced process technologies such as 40nm or below.

Advanced Field-Solver Technology, Better Accuracy, Capacity and Performance

Silicon Frontline's 3D technology eliminates the performance and capacity issues inherent in older Field-Solver technology and accomplishes full-chip extraction with Field-Solver accuracy. Typical examples of F3D running with *Guaranteed Accuracy* are a 65nm SOC run in under 10 hours; MOMCaps run in under 3 minutes, which takes over 7 hours with standard Field Solvers; and a 40nm design, where F3D delivered results within 2% of silicon, competing tools were up to 30% off. These results are not possible with commercial tools available today.

Technology, Users, Target Applications

The technology in Silicon Frontline's products is a combination of a rigorous 3D extraction method with a highly efficient 3D geometric engine yielding significant performance improvement and handling additional issues such as thickness variation due to CMP, width variation due to optical and other manufacturing effects. The software generates a fully annotated SPICE netlist with parasitics for use by downstream tools. It is used by CAD, TCAD and post-layout verification engineers.

F3D is ideally suited for sensitive analog and AMS circuits where coupling is a challenge – ADCs, DACs, circuits with differential signals, MIM/MOMCaps and 3D devices, image sensors, RF and high speed designs and for circuits manufactured at advanced technology nodes, such as 65, 40 and 32nm. R3D target applications include discrete or embedded power devices, where efficiency and reliability are important, as well as designs requiring analysis of large metal interconnects.

Price & Availability

F3D and R3D are available now. For information on pricing, please contact info@siliconfrontline.com.

About Silicon Frontline

Silicon Frontline Technology, Inc. provides post-layout verification software that is *Guaranteed Accurate* and works with existing design flows from major EDA vendors. Using new 3D technology, the company's software products improve silicon quality for standard and advanced nanometer processes. For more information please visit www.siliconfrontline.com.

Silicon Frontline Technology is headquartered at 420 Blossom Hill Road, Suite 202, Los Gatos, CA 95032, Tel: +1 408-356-3300, Fax: +1 408-356-3340. For sales inquiries or general assistance, please email info@SiliconFrontline.com.

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Notes to editors:
Pictures of the founders and product graphics are available by request.
Acronyms and Definitions

3D:	3 Dimensional
ADC:	Analog to Digital Converter
AMS:	Analog Mixed Signal
CAD:	Computer-Aided Design
CMP:	Chemical Mechanical Polishing
DAC:	Digital to Analog Converter
EDA:	Electronic Design Automation
MOMCap:	Metal–Oxide–Metal capacitor
MIMCap:	Metal-Insulator-Metal capacitor
Power Device:	Power devices are semiconductor devices used as switches or rectifiers in circuits for electronic circuits.
SOC:	System on Chip
TCAD:	Technology Computer-Aided Design