First Look

Silicon Frontline Aims at Post-Layout Verification

By Bill Murray

06/23/09

Founded in 2005, Silicon Frontline Technologies recently emerged from stealth to announce two products aimed at post-layout verification. This article delves deeper into the news, looking at accuracy, speed, design for power, and what's different about the tools, as well as tool testing and foundry qualification.

The first of the two products is F3D (Fast 3D) for fast 3D extraction. The second is R3D (Resistive 3D) for 3D extraction and analysis of large resistive structures, such as power devices. Both tools incorporate a patent-pending 3D technology that claims to deliver a "guaranteed accurate" solution for full-chip 3D parasitic extraction with performance equivalent to 2D tools.

F3D and R3D generate a fully annotated SPICE netlist with parasitics for use by downstream tools, and are targeted at CAD, TCAD and post-layout verification engineers who might otherwise build a test chip to measure critical silicon characteristics.

Using Fast 3D

According to the company, F3D is ideally suited for sensitive analog and AMS circuits where coupling is a challenge, such as ADCs, DACs, circuits with differential signals, MIMcaps/MOMcaps and 3D devices, image sensors, RF and high-speed designs. It is also applied to circuits manufactured at advanced technology nodes, such as 65nm, 40nm and 32nm. F3D leverages existing data required for current commercial extractors, such as process stack information, layer mapping and standard format for design data. According to the company, it integrates easily into existing standard physical verification flows, with support for texted GDSII as data input. Figure 1 illustrates where F3D operates in a typical flow.

© SCDsource 2007-2010

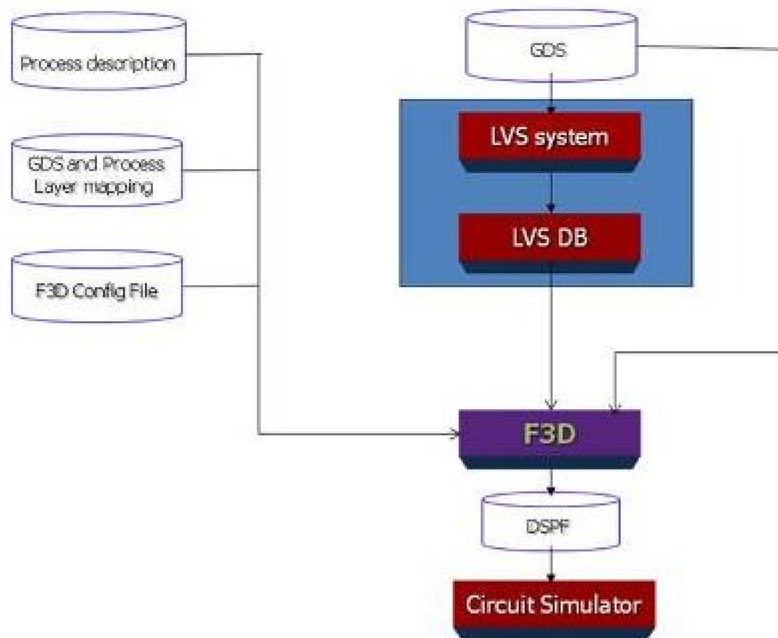

Figure 1: F3D in typical flow (Source: Silicon Frontline)

F3D reads in the GDS data, as shown in Figure 2, applies the process description information to it, and the tool’s database stores the resulting structure as shown in Figure 3.

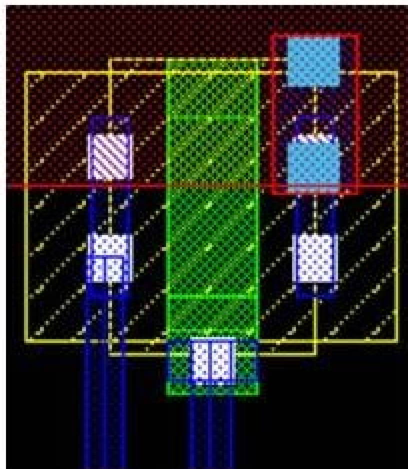

Figure 2: GDS data (Source: Silicon Frontline)

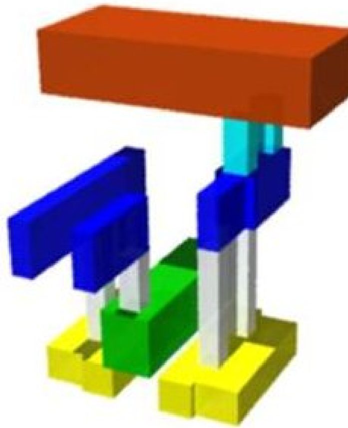

Figure 3: Representation in F3D database (Source: Silicon Frontline)

Accuracy and Speed

Silicon Frontline says that a unique feature of F3D is its ability to specify the extraction accuracy in the input and to trade-off the accuracy versus extraction time. The company claims F3D is significantly faster than the current 3D-accurate approaches, and that its convergence speed is independent of net size and layout complexity, unlike mesh-based systems. The company gave an example of running F3D on a metal-oxide metal capacitor (MOMcap). CEO Yuri Feinberg stated "With F3D, extraction took only 3 minutes, whereas another 'typical' 3D extractor took 7 hours to deliver the same accuracy."

What kind of results can first-time users expect? According to the company, although F3D is a 3D solver, its usage is similar to that of current 2D, 2½ D industry standard tools.

How does F3D accurately account for all of the 3D fringing parasitics significant in deep sub-micron technologies, such as boundary cut errors and extraction rule sets? VP of engineering Andrei Tcherniaev said that "F3D is a 3D field solver and is as accurate as any field solver available. There are, however, differences which can be very important in today's designs. F3D operates independent of a mesh, whereas traditional solvers depend on the quality of the mesh to obtain satisfactory accuracy. This is particularly challenging with advanced process technologies, which use very thin dielectric layers. F3D does not suffer from boundary cut off errors. It has the capacity and performance to extract full chip. This enables the end user to extract the design 'as is' without a trade-off between accuracy, capacity and performance. Users can therefore have a higher confidence in the quality of results (QoR) of the simulation."

Feinberg added, "Typically, today's designers run both 2½D (for performance) and 3D (for accuracy) tools, or in many cases simply build a test chip. For certain applications, such as image sensors or ADC, which require accuracy, F3D gives users the confidence that the parasitics are correct by handling the capacity and accuracy together." Feinberg illustrated his point with a real example: "An industry standard 2½D tool predicted that a 10-bit ADC would achieve 7½ bits of accuracy; F3D predicted 5 to 5½ bits, and the measured silicon was 5 to 5½ bits."

According to Feinberg, F3D's tight integration with industry standard physical verification tools enables it to derive full device and interconnect data. It can easily block out the

portion of the device parasitic which is already included in the SPICE model to avoid double counting. All fringing components, such as coupling from contact-to-gate and gate-to-diffusion, are properly extracted and can be optionally reported in a CCTG output file.

When asked to explain their claim of "guaranteed accurate", Feinberg said "Because our technology provides 3D field solver accuracy, the extracted values are within the accuracy level specified by the user, either net-by-net, at block-level or with regular expressions."

The company states that F3D is also capable of dealing with complicated embedded structures requiring 3D accuracy. Tcherniaev explained: "Complicated, intertwined, and closely packed metal structures (metal, via, contact, poly, and active layers) are typical in advanced silicon technologies. These structures make it necessary to comprehend three-dimensional capacitive effects. As an example, a parasitic capacitance from the poly gate of MOS transistors to source and drain nets is dominated by poly-to-contact capacitive coupling, which is an inherently three-dimensional effect."

To handle these effects, F3D builds the most realistic three-dimensional model of the nets, starting from standard input files (layout data and vertical BEOL stack description, specifying metal and dielectric thicknesses, dielectric constants, etc.), and performing complicated geometrical operations. This allows it to take into account both intended (as-drawn) 3D geometrical features, as well as non-trivial modifications to these shapes caused by so-called manufacturing effects – such as trapezoidal metal cross-sections, metal thickness variations due to CMP (chemical mechanical polishing), lithography effects, and dielectric etch damage.

Tcherniaev went on to explain that a complicated three-dimensional profile of the dielectric constant is also taken into account, featuring planar and conformal dielectrics, spacers, liners, and other details. A computational engine of F3D – random walk method – is a rigorous technique for solving the three-dimensional Laplace equation that characterizes the capacitive coupling between the nets. A floating random walk allows the tool to resolve both small and large features of the geometry, avoiding the need to build a huge three-dimensional mesh, and providing a very efficient way to extract the capacitance matrix.

According to Feinberg, "A very attractive feature of random walk method is that its speed of convergence does not depend on the size of the net. Another advantage is that the random walk technique automatically identifies nets with non-zero capacitive coupling to the net that is being extracted, which provides a natural 'filter' against large number of minute capacitances that clutter parasitic netlists in standard parasitic extractors, resulting in an unacceptably long circuit simulation time."

Design for Power with Resistive 3D

The company's second product, R3D, targets applications that include discrete or embedded power devices, where efficiency and reliability are important, as well as designs requiring analysis of large metal interconnects. Using R3D, power device designers who typically build a test chip to measure Rdson and to understand current density and switching loss issues, can have the results they need in hours. According to Silicon Frontline, a large IDM customer used R3D to achieve high accuracy results in hours rather than the months typically required to generate approximate results using other tools.

Silicon Frontline claims that R3D is the "only" tool capable of helping optimize power device design, which is critical for automotive, industrial and consumer applications.

© SCDsource 2007-2010

"Power issues addressed by various current EDA tools are developed for standard digital and analog circuits," stated Tcherniaev. "In these circuits, a huge number of elements, each consuming a relatively small amount of power, results in a large total power consumption. In contrast, a power device addressed by R3D is a single device of very large size – up to several square millimeters – and a wide gate. These devices include metal-oxide-semiconductor (MOS) transistors, double-diffused MOS (DMOS), lateral DMOS (LDMOS), vertical DMOS (VDMOS), trench MOS, and other types of transistors able to sustain very high blocking voltages – up to several hundreds of volts – and have a very low on resistance from several Ohms to several milliOhms."

According to Feinberg, "The experience of over twenty customers – power and analog semiconductor companies – has demonstrated that the standard parasitic extraction tools yield skewed Rdson values, inconsistent trends, and cannot visualize current flow and analyze current density distributions." He added that the size of the parasitic netlist generated by standard extractors for power devices leads to unacceptably long simulation times by general-purpose SPICE simulators. A deep integration of R3D's extraction, geometry processing, meshing, and linear solver technologies achieves accurate results with modest computer resources.

Tcherniaev explained that discretization of the current transport equation on a detailed two- and three-dimensional mesh automatically guarantees resolution of non-uniform current effects, such as spreading of the current, current crowding in narrow metal regions, or in edge or corner vias of via arrays, non-uniform current flow in the device array, and potential drop on resistive elements. According to Tcherniaev, R3D provides an efficient post-processing tool that allows it to visualize current density and potential distributions, to highlight the areas with current densities (for electromigration analysis), and to capture bugs and errors in layout that are very difficult to identify just by visual inspection.

The tool reads in standard files describing device layouts (metal, via, contact, and device layers) and vertical BEOL (back-end-of-line) stack (specifying metal thicknesses, resistivities, etc.) in order to build a three-dimensional representation, or database, of the device structure. Subsequent geometrical processing and generation of a finite difference mesh are used to discretize the current transport equation (Laplace equation) in metal nets and devices. The discretized equations are solved using a proprietary linear matrix solver to obtain the solution (potential and current density distributions, Rdson value, etc.).

What's Different?

According to the company, current tools fail to handle a number of key issues correctly, leading to inaccurate post layout verification. Feinberg cited some examples:

- Non-uniform current flow, which impacts the accuracy for power devices such as DC-DC converters, and for multi-finger devices in high-speed design.
- Metal fill that causes errors in capacitance extraction values.
- Manufacturing effects that cause inaccuracy in capacitance and resistance extraction.
- Device-to-device capacitance that leads to underestimation of total capacitance and inaccurate values of coupling capacitance.
- Huge parasitic netlist files that can lead to excessive circuit simulation time.
- Very long database generation time (up to a week) for pattern matching extraction tools.
- Problems with "blocking" device capacitances.
- Problem in decoupling active device and parasitic capacitances.

© SCDsource 2007-2010

SCDsource pointed out that chip companies are, in fact, delivering chips to market, despite these apparent problems with current tools. Feinberg responded, "In general, it's true that IC design houses have successfully used existing solutions for designing chips. However, they are well aware of the limitation of current tools and design around these issues. Some design styles, such as image sensors and ADC converters, require high accuracy with capacity. Furthermore, some of the issues which were ignored in older technologies must be addressed at advanced technology nodes. An example of this is the coupling between contact and gate (CCTG)."

Adopting and Using the Tools

Feinberg states, "Unlike the current 'state-of-the-art' 3D field solver solutions, which require propriety format for input, F3D leverages existing data for input and provides a distributed RC SPICE netlist (DSPF) for output, that can be used by circuit simulators."

In addition to accepting standard input and output formats, F3D requires no modification to the input data, and supports all manufacturing effects for advanced process nodes such as thickness and width variations, temperature dependent R, and layout scaling. This information is available as input in the process technology files. An example of this file format is iRCX from TSMC.

Tool Testing and Foundry Qualification

At present, F3D is qualified at TSMC and UMC for the 65nm, 45nm and 40nm technology nodes. F3D has been correlated with measured data using advanced process technology with test structures, finger devices and ring oscillators.

To achieve qualification with TSMC and UMC, F3D was tested and compared to measured silicon and industry standard 3D extraction results. The correlation to 3D extractors required extracting a very large number and range of structures. Correlation with measured silicon required running a range of circuits including PLLs, ADCs and inverter chains. In all of these tests, F3D results were always within a few percent of the measured silicon. Additionally, at IDMs and fabless customers, F3D has been correlated using a 65nm SOC, multiple image sensors, ADCs and high speed I/Os.

R3D has been thoroughly tested using both analytical solutions on simple geometries and silicon data on practical designs. R3D predicts accurately both absolute values of Rdson (the on-resistance of power device), and Rdson trends versus layout or metal resistivity changes. The difference between R3D results and measured Rdson values is approximately 5 percent, and is achieved without any fitting of simulation results to experimental data. According to Silicon Frontline, this is an excellent agreement, given the fact that the individual components of Rdson – such as device compact model, metal thicknesses and sheet layer resistivities – can vary by as much as 10 to 15 percent due to process tolerances.

Verification of R3D accuracy has been performed using the data from over 20 customers – power and analog semiconductor companies, IDMs, foundries, and startups – on about 80 different designs With different power device types and layout styles, such as MOS, DMOS, VDMOS and LDMOS devices with rectilinear, oval, mesh, and meander gate layouts.

© SCDsource 2007-2010